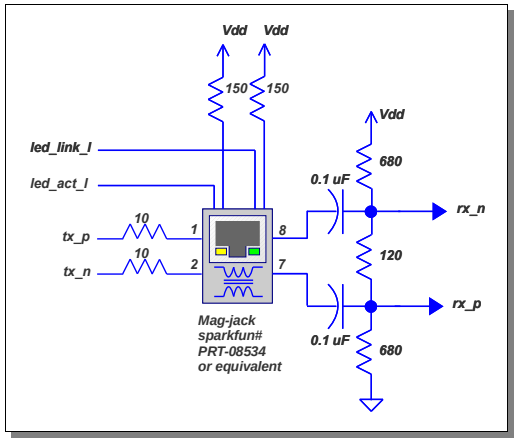
WebPHY DATABUS

Quick-Start Guide

1. Connect the hardware

Use the following circuit to wire a Digilent Spartan-3 Starter Board to a RJ-45 mag-jack. Connect the mag-jack to a switch/wireless router using a standard CAT5 Ethernet cable.



Signal	Digilent Board	FPGA Pin
gnd	A2-1	n/a
rx_p	A2-12	C8
rx_n	A2-13	D8
vdd	A2-3	n/a
tx_n	A2-9	E7
tx_p	A2-11	D7
led_act_l	A2-20	A5
led_link_l	A2-19	B5

2. Get the tools

Download and install Xilinx ISE 14.7 and Strawberry Perl.

3. Build and download

Power on the FPGA and run s3_digilent.bat in the scripts directory. This batch file generates the web page BRAM from web sources, creates an ISE project, and builds and downloads the project to the FPGA.

When the download completes, verify that the 7 segment display reads “8000” and that the green LINK LED illuminates solid. The amber ACT LED may flicker indicating the presence of traffic.

4. Access the web page

Use a PC smartphone or tablet to navigate to **http://192.168.1.5**, and log onto the FPGA. Verify that clicking the red ds0-7 LEDs illuminates the corresponding LEDs on the Digilent board and that the slider changes the number displayed on the 7 segment display.

5. Add a button

Add the following code to /web/html/index.html:

```
<BR>
<button onclick='cmd("wr,0x0,0x1234")'>Servo 0x1234</button>
<button onclick='cmd("wr,0x0,0x5678")'>Servo 0x5678</button>
<button onclick='cmd("wr,0x10,0xAA")'>LEDs 0xAA</button>
<button onclick='cmd("wr,0x10,0x55")'>LEDs 0x55</button>
<BR>
```

Run scripts/romgen.bat to regenerate the initialized BRAM file /src/webram.vhd for synthesis and the instant-upload file /out/webupdate.txt.

On the core's web page click Browse to select /out/webupdate.txt and click Upload to send the modified web page image to the FPGA. When the upload completes, the web page will automatically refresh. Verify that the new buttons have been added and clicking them controls the LEDs and servo+7-segment display. Try modifying other html, js and css sources referenced in index.html.

6. Add a register

Add the following line to the wr_regs_proc in /src/user_logic.vhd:

```
when X"100" => customreg <= wr_dat;
```

Rebuild the FPGA and type “wr 0x100 0xAB” in the command box on the web page to write 0xAB to the custom register.